Additional Degree of Freedom in Interleaved Junction Silicon Modulators against Efficiency-energy Conflict

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Abstract: This paper introduces lateral contribution into interleaved junction. Numerical analysis suggests light-carrier overlap enhancement. VπLπ and energy consumption can both surpass lateral junction performance as opposed to conventional interleaved junction suffering from efficiency-energy conflict.

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Interleaved junctions can achieve better modulation efficiency (VπLπ) than lateral junctions in hope to reduce phase shifter length as well as insertion loss. However, the energy consumption actually increases since the capacitance is higher due to inefficient junction interfaces away from waveguide center [1, 2]. Improving light-carrier overlap is the most straightforward solution. Although interleaved junction widths larger than [1], smaller than [3], or equal to [2, 4] the waveguide width have been demonstrated, this issue remains unsolved, and dopants straggling into the slab region also form unwanted lightly doped junctions that adds to the total capacitance. In this paper, lateral junction is introduced as an additional degree of freedom to enhance light-carrier overlap and eliminate the detrimental capacitance from straggling. The results now promise both lower energy consumption and VπLπ than conventional lateral junctions.

Compared with conventional interleaved junction [Fig. 1(a)], the proposed junction [Fig. 1(b)] incorporates an additional junction at the end of interleaved shape, and the lateral parameter (offset) now determines the lateral junction position as well as the interleaved junction width. Therefore, a small offset enhances the lateral contribution by placing the junction closer to the waveguide center, but resulting in a narrower interleaved junction width. This implies an appropriate offset should maximize the light-carrier overlap and thus minimize energy consumption. Note that a trade-off now exists, as opposed to conventional interleaved junction where larger offset always leads to lower energy consumption. 3D simulation is usually required to account for the heterogeneity along the propagation direction. However, the absolute error of effective index change per unit length per unit length (Δn_{eff}) ~10^{-6} cannot be obtained with reasonable time complexity. To address this issue, an analytical characterization method of Δn_{eff} is proposed using 2D simulation obtainable parameters: interleaved junction contribution Δn_{i} and lateral junction contribution Δn_{l}. The 2D simulation validity is verified by comparing with published results that model basic junctions and experimentally verified the simulations [5]. Since junction depletion only exerts perturbation (Δn~10^{-3}) on the mode profile, the total contribution to Δn_{eff} can be written as:

$$\Delta n_{eff} = \frac{1}{2L_{pitch}}\left(2\Delta \mathrm{n}_i(offset)\Delta w + \Delta \mathrm{n}_l(offset)L_{pitch} + \Delta \mathrm{n}_l(-offset)L_{pitch}\right) \quad (1)$$

where L_{pitch} is the doping size and Δw is the width change of depletion region. Results of Eq. (1) are numerically shown in Fig. 1(c-f) for L_{pitch}=210 nm (CMOS 90 nm node) and Fig. 2 for L_{pitch}=300 nm (CMOS 130 nm node). The interleaved contribution grows with offset (junction width), and energy consumption reaches minimum at max offset of 225 nm, which is the physical principle behind conventional interleaved designs. However, the energy consumption is higher than that of the optimized lateral junction (green lines), especially for 300 nm pitch [Fig. 2(b)]. The red lines show the additional lateral junction contribution in the proposed junction. Notches at offset ~170 nm [Fig. 1(a), Fig. 2(a)] are observable, causing a slight decrease in total Δn_{eff}. This is because at this offset, depletion region extends into the slab and light-carrier overlap significantly drops, indicating that a greater offset will be much less efficient. The additional lateral contribution now changes the physical pictures: both VπLπ and energy are not necessarily optimal at max offset. Fig.2 (c) suggests [Energy, VπLπ]=[5.58 pJ/bit, 0.74 V·cm] at offset=170 nm for best VπLπ and [5.11 pJ/bit, 0.82 V·cm] at offset=90 nm for lowest energy. More importantly, Fig. 1(e) (L_{pitch}=210 nm) indicates that at offset=160 nm, modulation efficiency and energy of [4.31 pJ/bit, 0.60 V·cm], both outperforming the lateral junction [4.97 pJ/bit, 1.02 V·cm] can be obtained. The underlying physical concept is that the additional lateral junctions enhance light-carrier overlap in the waveguide core and reduce inefficient

junction capacitance near the edges. The idea of introducing additional junction components provides new possibilities of simultaneous demands on low modulation energy and high efficiency.

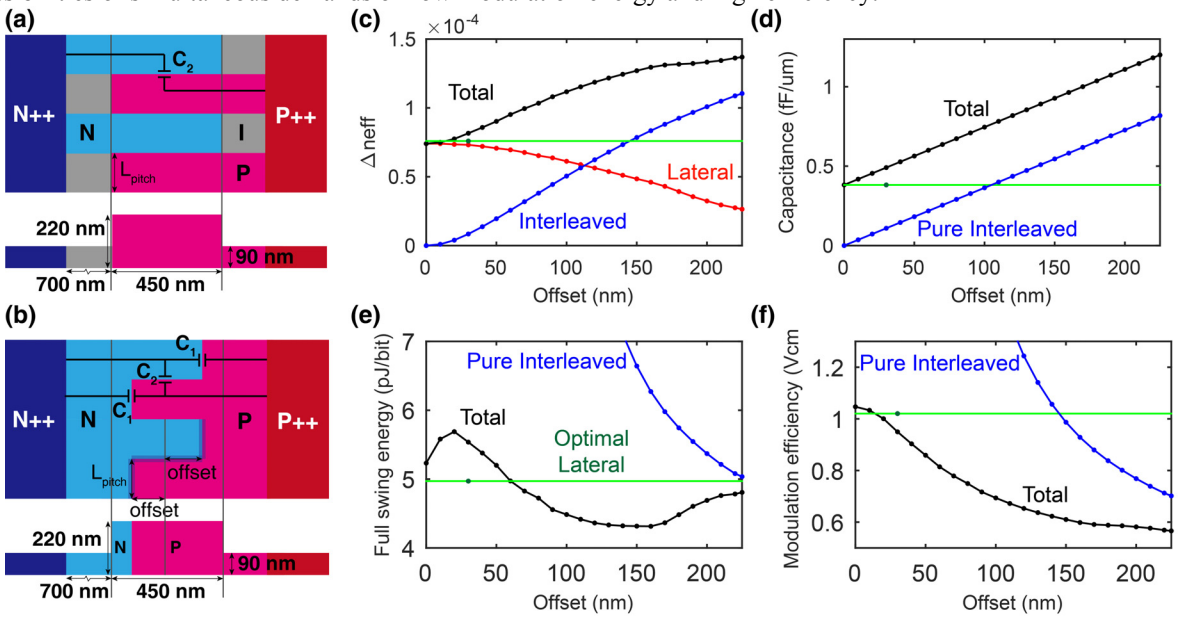

Fig. 1. Schematic of (a) conventional interleaved junction and (b) the proposed junction, top-view and cross-sectional view. (c-f) analysis of (c) Δn_{eff}, (d) junction capacitance, (e) energy consumption and (f) modulation efficiency. Energy calculation assumes 1-mm long phase shifter and push-pull modulation of full transmission swing (0-1). L_{pitch}=210 nm matches CMOS 90 nm node capabilities. Doping parameters in this work are 5×10^{17}/cm^3 and 1×10^{18}/cm^3 for P and N doping, 10^{20}/cm^3 for heavy doping. To comply with corresponding doping feature size, offset≥105 nm can be fabricated without violation of design rules.

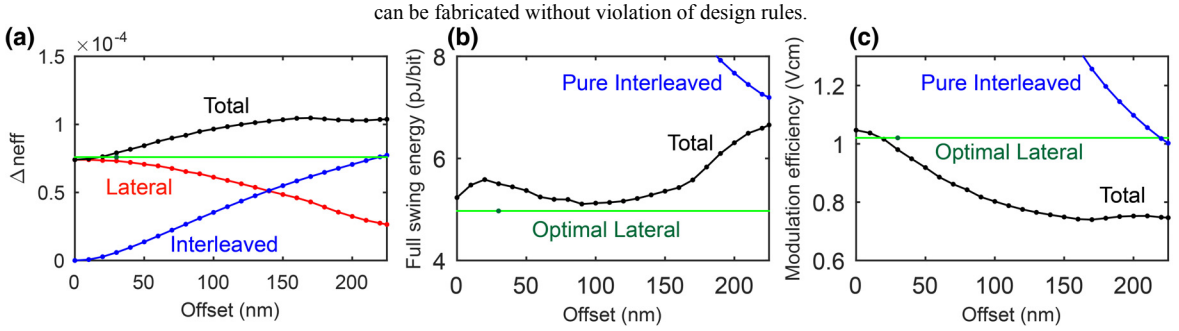

Fig. 2. Analysis of (a) Δn_{eff}, (b) energy consumption and (c) modulation efficiency. Different from Fig. 1, L_{pitch}=300 nm is analyzed, which is available in commercial foundries. Offset≥150 nm can be fabricated without violation of design rules.

Lateral contribution is introduced to interleaved junctions as an additional degree of freedom to enhance light-carrier overlap and mitigate efficiency-energy conflict. Numerical analysis shows that the light-carrier overlap is enhanced and max offset is no longer preferable as opposed to conventional interleaved junctions. Modulation energy and efficiency both outperforming conventional lateral junction are observed, suggesting new possibilities to meet stringent requirements on both energy and VπLπ. The proposed modulator junction design is highly favorable in applications such as optical communications and interconnects.

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