CMOS as a Research Platform

Microelectronics Research Center

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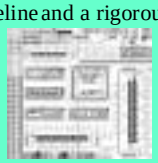
Georgia Institute of Technology

Platform

To facilitate research on a variety of new materials, device structures, and microelectromechanical systems, the Microelectronics Research Center of Georgia Tech has established a silicon CMOS processing baseline and a rigorous procedure for equipment and processing training. The Platform is open to the entire Georgia Tech community and to other research communities around the world.

The Platform consists of five integrated components: Baselines, Research, People, Training, and Service.

In the future, the baseline will include:
- A complete 1 micron, twin-well, double metal, double poly technology
- Support for nanotechnology research



2 Poly, 2 Metal, N -well CMOS Circuits

CMOS Circuits on 4" wafer

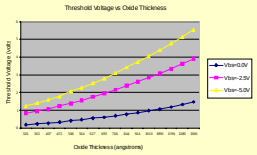
1 micron P-MOS device

Baselines

Three baselines, hosted in a 7,000sq. ft. class 10-100 cleanroom and capable of 4"-6" wafer production, have been established at the Microelectronics Research Center:

- 20 µm NMOS and CHEMFET
- 2.5 µm P-well, single metal, single poly
- 1.3 µm N-well, double metal, double poly

The baselines include process simulation, circuit design, mask generation, a set of processing equipment and recipes, and a set of test and measurement instruments. The processing equipment includes horizontal diffusion furnaces, MA6 mask aligner, sputterers, spin coaters, RCA clean station, rinse and dryer, pattern generator, stepper, ICP etcher, RIEs, PECVDs, evaporators, and a Hitachi S-3500H SEM.



$$C(acc) \cong C_o = \frac{K_s \varepsilon_o A_G}{\chi_o}$$

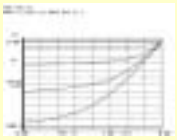
$$C(depl) = \frac{C_o}{1 + \frac{K_s W}{K_o \chi_o}}$$

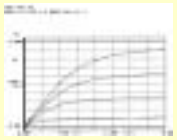
$$C(inv) = \frac{C_o}{1 + \frac{K_s W_T}{K_o \chi_o}}$$

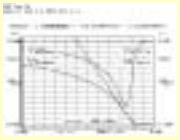
$$C(inv) = C_o$$

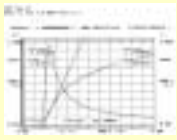
$$V_G = \phi_s + \frac{K_s}{K_o} \chi_o \xi_s$$

MOSFET Simulation







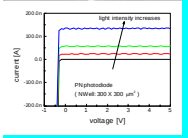


I-V curves of 1.3 µm CMOS transistors

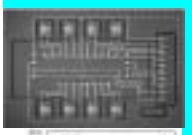
Research

The Platform supports collaboration and a variety of research, which includes, but is not limited to, the following programs:

- Nanofabrication
- Novel CMOS structures
- Chemical sensor array
- Electronics for MEMS
- Integrated optoelectronics
- DNA chip array
- New interconnection schemes
- Sea of Leads chip input/output interconnects



Si Photodiode

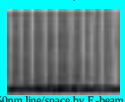


GT-01
chemical sensor array
exposed to ammonia

Poly membrane on air gap

400nm HTO by LPCVD

350nm lines by MA-6



150nm line/space by E-beam

People

Gary Spinner and co-op student David Sigmon are checking the equipment

Bob Rose is supervising co-op student Siddharth Jain

Training

The Platform provides a rigorous equipment and processing training program for new cleanroom users.

- Training procedure:

Orientation, onsite equipment training, one -on-one check off, and processing training and consultation.

- Databases:

Equipment operation instruction database

Process recipe database

- Training capacity:

16 classes per month, 8 students per class

- Trainers:

MIRC staff, graduate students, student assistants

- Accomplishment:

500 classes, with over 3000 attendees, conducted between Sept. 1999 and Dec. 2002.

Group Training

One-on-one check-off

Services

The Platform provides the following processing services to the Tech research community and other research groups around the world.

CMOS Runs (Quarterly)
- Process design
- Mask design
- Processing
- Characterization

Co-op student Aric Madayag is performing Wet/Dry oxidation

Process Modules Run (as needed)
- Wet/Dry oxidation
- LPCVD nitride growth
- LPCVD polysilicon growth
- RIE nitride and poly etch
- Optical lithography
- Multilevel interconnection
- Any combination of above