The final report on batch 14 CMOS run (high yield) at GT MiRC

James Zhou
November 30, 2004

I. Prior to a new run

Five major equipment related issues have been identified as the possible causes for low yields from our previous CMOS runs:

1. Reduction of ICP processing selectivity between SO2 and Si to 1:1 (previously ~11:1);
2. Possible plasma damage to the gate area from strong ICP power;
3. Overlarge polysilicon grain size;
4. Overlarge aluminum grain size;
5. Cross contamination from other non CMOS compatible sources.

The first four issues have been addressed and tested as follows:

1. Use of RIE instead of ICP machine (same recipe) to obtain high etching selectivity between SiO2 and Si;
   - The same recipe (as used in ICP) produced a satisfactory selectivity result by using RIE machine: about 10:1 = SiO2: Si, which is very close to the selectivity obtained from ICP machine at the old good time.
   - Since RIE is heavily used and shared equipment, a special shower plate was designated for CMOS processing and a necessary gas was scheduled for CMOS processing at certain days of the week.
   - A two step process has also been introduced to prevent heavy polymer deposition during the contact cut process. The two step process has been producing consistent and satisfactory results: about 7700A SiO2 etched but 150A into Si.
2. Use of STS ICP at lower power level to etch poly gate;
   - Lower power level extended the etching time. About 3 minutes to clear 4500A poly with great uniformity. No physical damage to gate oxide found by AFM.
3. Use of a clean tube before depositing polysilicon layers for CMOS;
   - Every time the tube was cleaned, less than 3% of non-uniformity across the wafer was achieved.

4. Use of slower deposit rate to deposit Al.
    - Slow deposit rate (200A/min) produced a uniform and fine Al layer. Electrical testing, Optical inspection, and SEM observation all point in the direction of a very good Al film.

Issue No. 5 has not been resolved due to limited resources in the clean room. A written proposal: "Classifications of MiRC Processing Equipment", which may solve issue no. 5, was sent to MiRC management for consideration on Oct. 11, 2004.

II. Current CMOS run (Batch 14)

A new CMOS run "Batch 14" was started in April 2004. Care was taken to refrain from product wafer processing unless (1) the equipment was ready and well calibrated through test processes, and (2) the previous product wafer processing step was well measured and characterized. This strategy worked well except that it stretched the run period to much longer than usual as most of the equipment was not calibrated and the current equipment scheduling system prevented the formation of a seamless CMOS processing flow.

During the course of the front end processing, a few equipment breakdowns (Nitride tube: 6 days, Oxide tube: 8 days, Poly tube: 4 days) stalled the process. By the time the front end processing steps were finished, all the tests and measurements were inline with expectations, except the N+ implantation process shrank our photo resist. Particularly, the uniformity across the wafer is very satisfactory.

For the back end processing, starting at the "PSG deposition" step, most steps went smoothly except the RIE and metal deposition equipment, which broke down for a few days. The RIE also contributed to the non-uniformity both across wafers and from wafer to wafer (a RIE run produced two strange "bars" on each wafer) because the RF power supply and its matching network had a few problems. The back end processing stopped right before the metal 2 deposition because the rough surface of the spin-on-glass (after VIA etch) was unable to support a smooth enough metal 2 layer. Since the absence of the metal 2 layer does not distort the test data, the results and analysis presented in this report reflect the quality of the batch 14 CMOS run at GT MiRC.

The measurement and testing takes longer than usual, too, since the old hard drive of the controlling and data collection computer failed during the testing and disrupted the testing program software and setup. It took about 3 weeks to bring back the testing system.

III. Test results and analysis

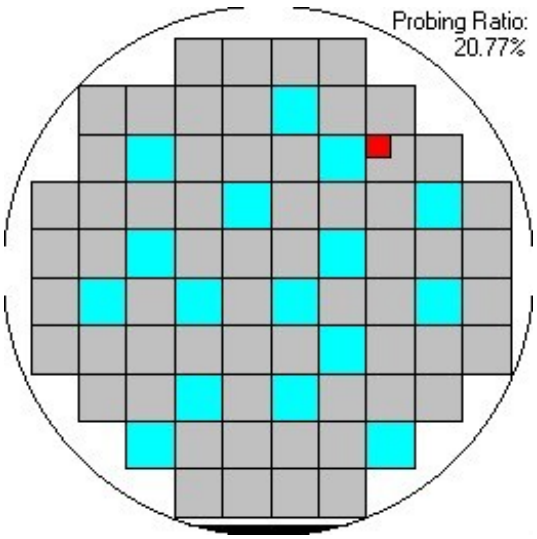
The batch 14 started with 9 wafers, but 2 of them were lost during metal 2 deposition and the following wet Al etching processes. Therefore, only 7 wafers (wafer 1, 2, 3, 4, 5, 7, and 8) and 16 dies on each wafer were completely tested. The total 17 electrical parameters on each die were tested. These parameters are:

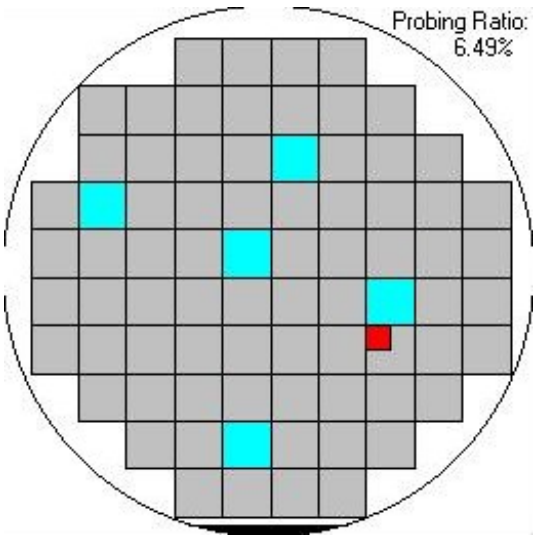
N+, P+, Poly Metal1 sheet resistance;
N+, P+, Poly contact resistance;
N+, P+, Poly contact chain resistance;
Metal1, Poly CD;
Metal1, Poly comb leakage;
Metal1, Poly serpentine resistance;
NMOS & PMOS Threshold Voltage

As part of preliminary testing, the threshold voltages, I-V curves, and other electrical parameters of the wafer 6 and 9 were tested on 5 different dies before the Spin-on-Glass step.

The reliability test, Bias Temperature Stress Test, is still waiting for the equipment upgrade. In order to perform a complete "Biased Temperature Stress (BTS) Test" (Applying bias at 300C for a few hours) for our CMOS devices, a special chamber, adapter, probe holders, cables and other high temperature components are needed. A recent price quote from Cascade MicroTech, about $4,132, was sent to MiRC management on November 23, 2004 for approval.

The 16 die and 5 die test maps with the location of tested dies are shown below.





The test results presented in this report are in four different groups: (1). wafer by wafer electrical test results, (2). wafer by wafer threshold voltage results, (3). combined electrical test results of 7 wafers, and (4). data from wafer 6 and wafer 9. Group 1-3 results are taken from wafers 1, 2, 3, 4, 5, 7, and 8, and group 4 is the preliminary report based on wafers 6 and 9.

Group 1. Wafer by wafer electrical test results

See Appendix A. From the following graphics, one can easily conclude that the results are mostly within the control limits and uniformly distributed across the wafer. The yields (pass rates) of each tested parameter are very high **(mostly at 81%, 88%, 94% or 100%)** compared to previous CMOS runs. The uniformity from wafer to wafer is also excellent.

> Note: the structure of W/L = 10/5 microns is used for the threshold voltage test.

Group 2. Wafer by wafer threshold voltage results

See Appendix B. The target threshold voltage for the W/L = 10/2 microns structure is +/- 0.75 volts. The following graphics show that they are very well maintained, across wafers and from wafer to wafer, and for different W/L ratios **(mostly 100% pass).**

Group 3. Combined electrical test results of 7 wafers

See Appendix C. This group of graphics shows the comparisons of each parameter on all wafers.

Group 4. Preliminary report based on wafers 6 and 9
See Appendix D. This group of data includes some images from an optical microscope, and test results of the threshold voltages, I-V curves, and other electrical parameters from wafer 6 and 9 right after metal 1 process.

IV. Conclusion

The significantly improved yield in this batch 14 demonstrated that as long as (1). the processing and testing equipment were ready, calibrated, and well maintained, and (2) that adequate resources are available, an excellent CMOS run with high yield can be obtained by using the **CMOS as a Research Platform** at MiRC of Georgia Tech.

V. Contributors

The students contributed to the Batch 14 CMOS run are:

Leslie Oommen George
Matthew Leidy
Biren Patel
Arun Rambhatla
Peter G. Sahlstrom