MiRC CMOS Batch 14 Preliminary Report

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September 24, 2004

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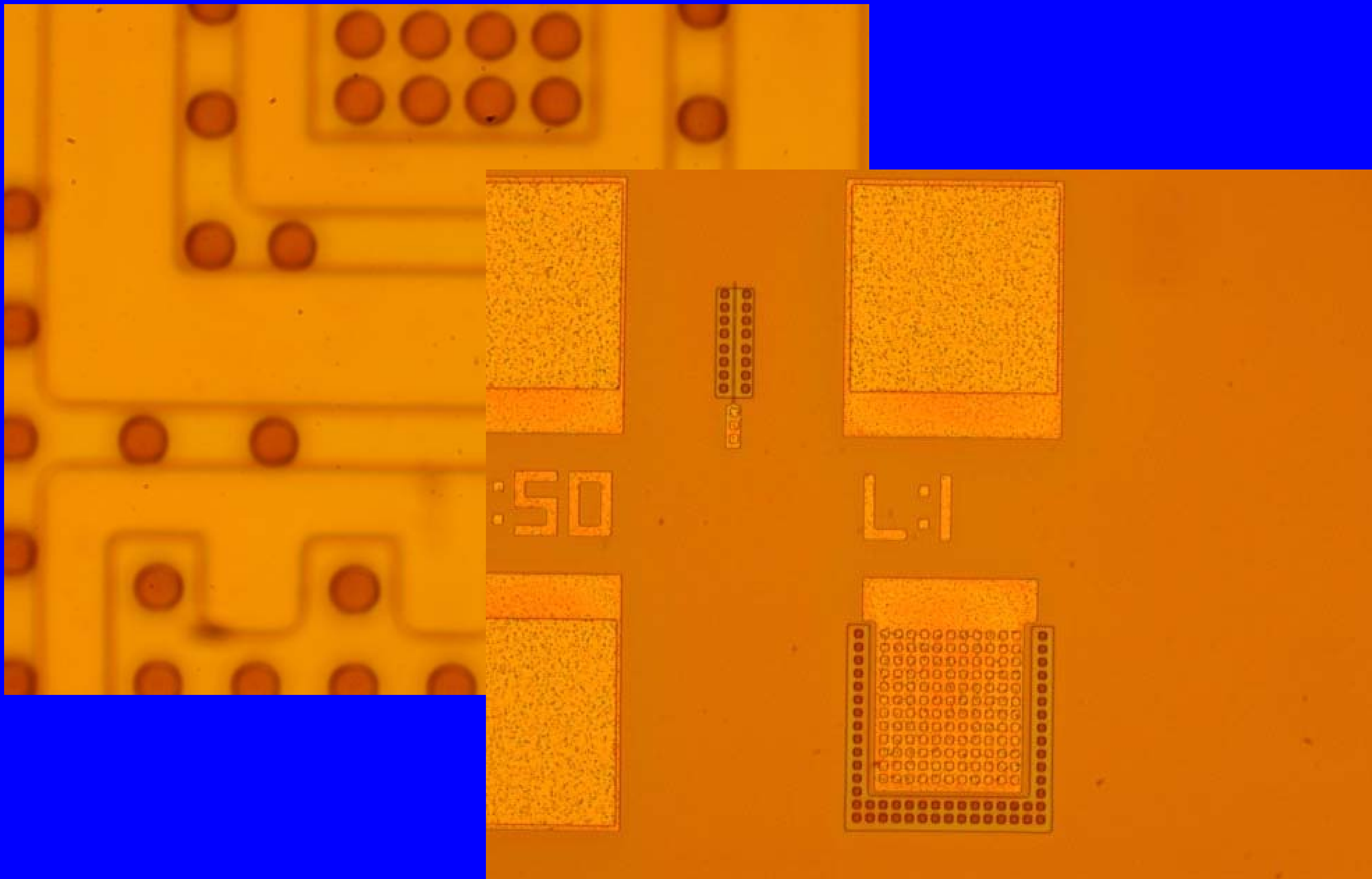
Outline

- Processing the Batch 14
- Individual Transistor Test
- Semi-complete Electrical Test
- Online Resources
- Challenges

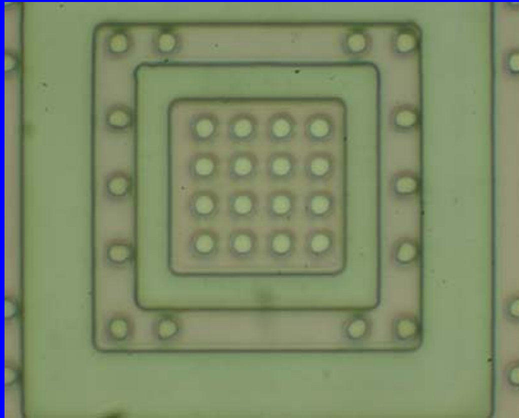
CMOS Batch 14

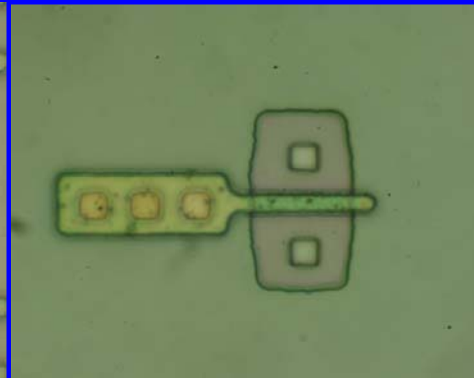
- *2 micron, 2 poly, 2 metal, N-well technology*
- *Contains only CMOS test structures and test circuits*
- *Started in April and finished Metal 1 in August*

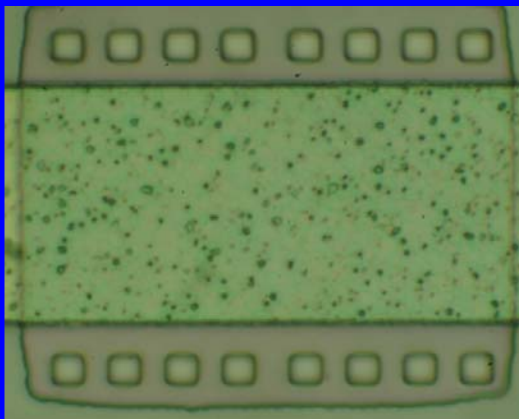
Contact Photo

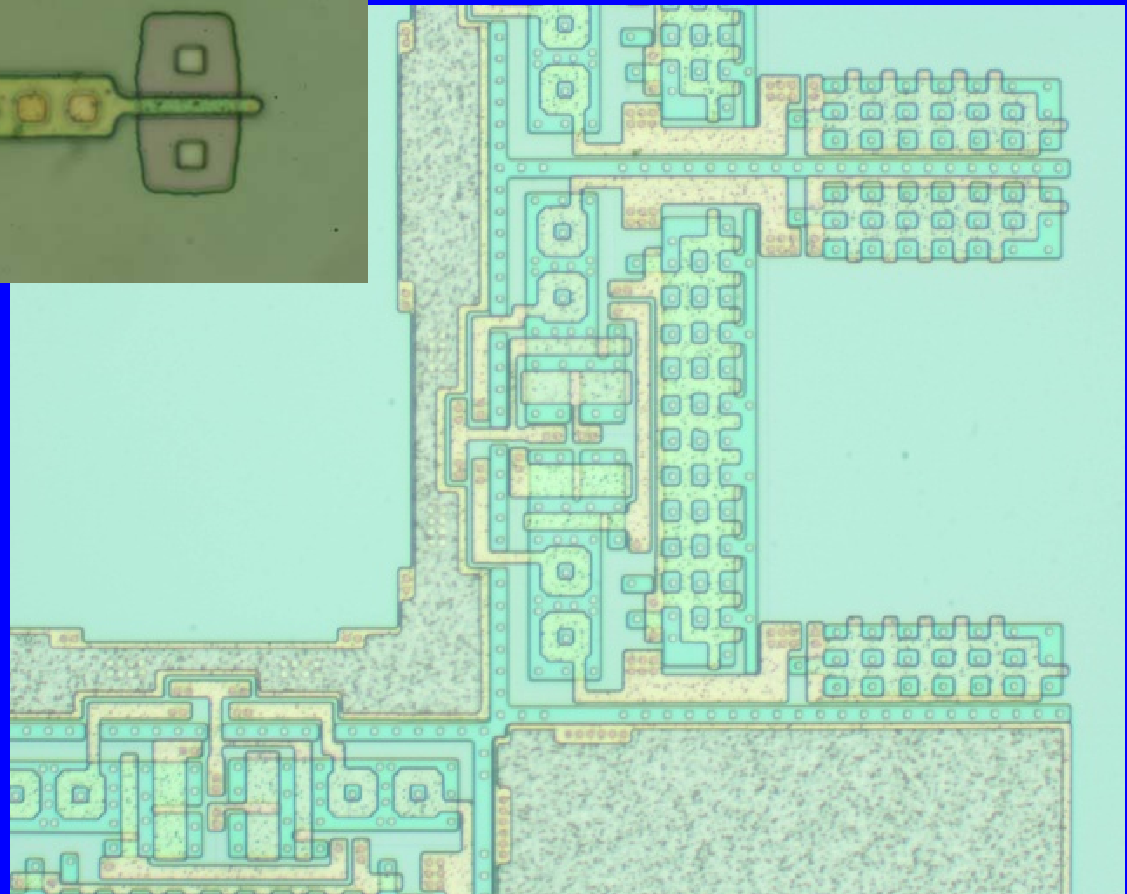


Contact Etch

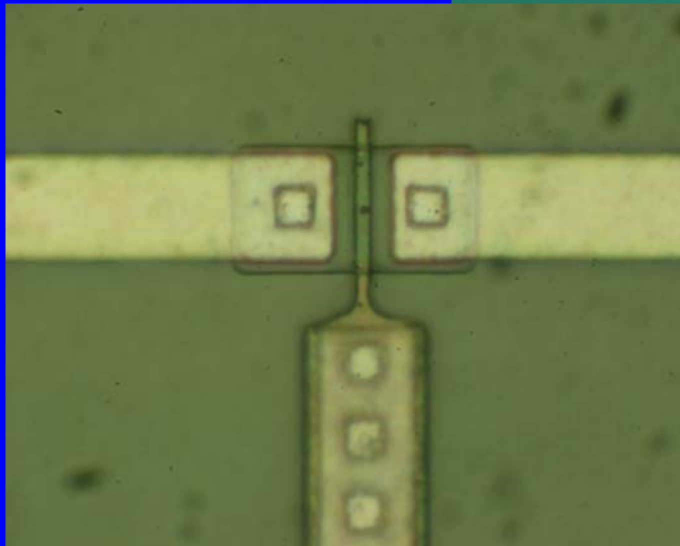








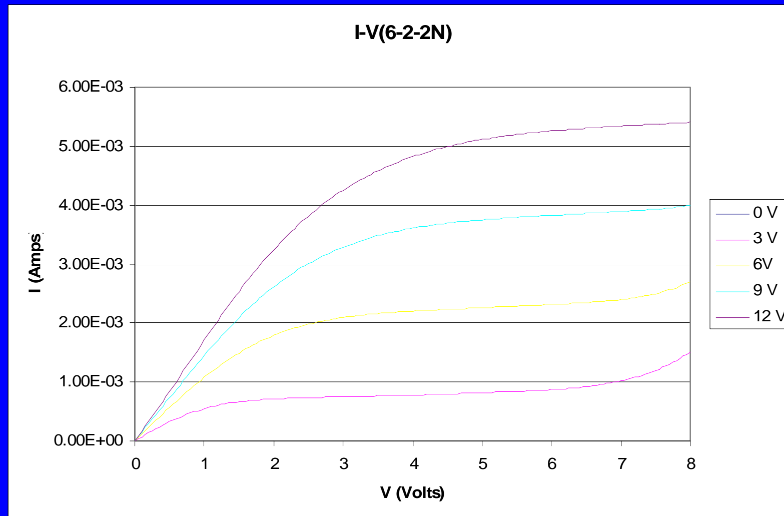
Via Etch

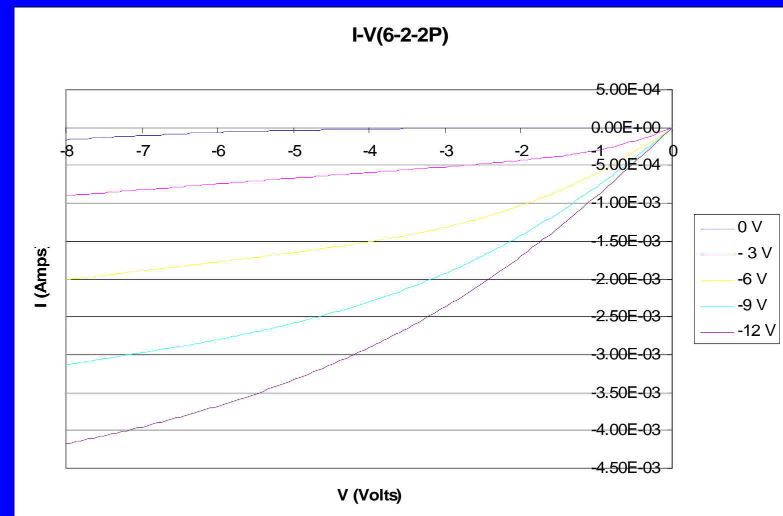


Individual Transistor Test

- *NMOS and PMOS*
  - *L=2 micron and W=10 micron*
  - *Targeting thresholds: +/- 0.75V*

Wafer 6, Die 2

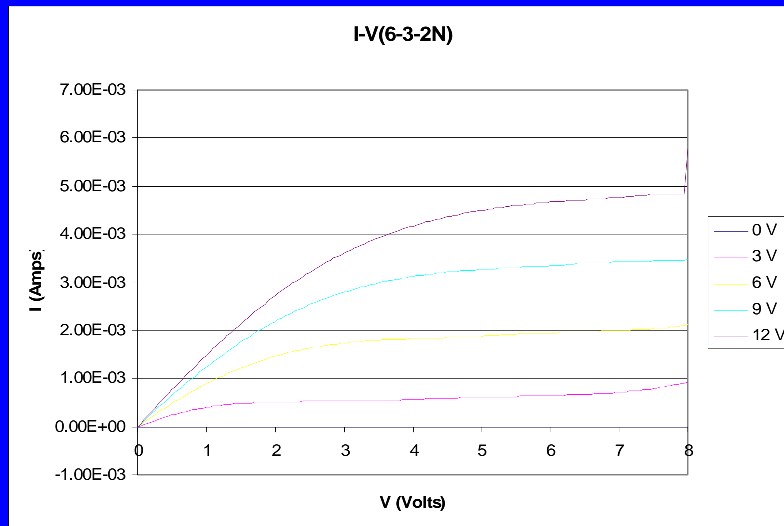


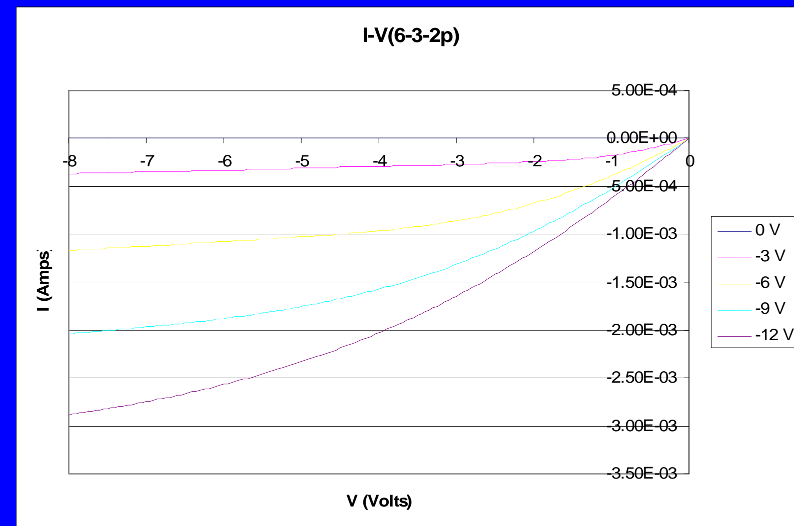


Vth=0.497 V

Vth=-0.538 V

Wafer 6, Die 3





Vth=0.45 V

Vth=-0.728 V

Semi-complete Electrical Test

- *Variety of tests:*

  N+, P+, Poly Metal1 sheet resistance
  N+, P+, Poly contact resistance
  N+, P+, Poly contact chain resistance
  Metal1, Poly CD
  Metal1, Poly comb leakage
  Metal1, Poly serpentine resistance
  NMOS & PMOS Threshold Voltage

Die Position	N+ Sht R(Ohms)	P+ Sht R(Ohms)	Poly Sht R(Ohms)	Poly Cd(um)	Poly Comb Lkge(Amps)	Poly serp R(Ohms)
7,5	33.04849885	47.69585253	21.23502304	2.885967897	1.91E-11	9.96E+04
4,6	32.00923788	46.86635945	20.93087558	2.943404378	1.72E-11	9.36E+04
1,7	37.20554273	52.88018433	21.51152074	3.32525416	4.50E-03	8.70E+02
5,7	34.29561201	49.14746544	20.35023041	3.169939738	1.61E-11	8.54E+03
Mean	34.13972286	49.14746544	21.00691244	3.081141543	1.75E-11	6.72E+04
Stddev	2.247464423	2.661065883	0.497887828	0.203748512	1.51767E-12	50929.89823
Min	32.00923788	46.86635945	20.35023041	2.885967897	1.61E-11	8.54E+03
Max	37.20554273	52.88018433	21.51152074	3.32525416	1.91E-11	9.96E+04
%Yield	100	100	100	100	75	75

Wafer 6

Poly Cnt Chain R(Ohms)	M1 Sht R(Ohms)	M1 CD(um)	M1 Comb Lkge(Amps)	M1 Serp R(Ohms)
2.08E+03	45.17910608	1.96814282	1.41E-10	112
2.04E+03	45.31505123	2.92960363	3.56E-02	103
2.86E+03	48.03395431	3.16587426	3.27E-11	107
1.07E+03	44.90721577	2.86671849	3.74E-02	98.7
2.01E+03	4.59E+01	2.73E+00	8.69E-11	105.175
733.001819	1.459960655	0.52564867	7.65797E-11	5.673549741
1070	44.90721577	1.96814282	3.27E-11	98.7
2.86E+03	4.80E+01	3.17E+00	1.41E-10	112
100	100	100	50	100

N Vth(V)	P Vth(V)	N+ Cnt R(Ohms)	N+Cnt Chain R(Ohms)	P+ Cnt R(Ohms)	P+ Cnt ChainR(Ohms)	Poly Cnt R(Ohms)
0.599	-0.763	79.4	1.04E+04	125	1.76E+04	3.38
0.615	-0.738	80.4	1.04E+04	70.3	1.05E+04	2.76
0.645	-0.774	168	240	133	9.52E+03	16.7
0.602	-0.774	74.8	9.93E+03	65.6	9.89E+03	2.51
0.61525	-0.76225	100.65	1.02E+04	98.475	11877.5	6.3375
0.021013884	0.016977927	44.96617247	271.3546265	35.45018806	3836.338315	6.9180073
0.599	-0.774	74.8	9.93E+03	65.6	9520	2.51
6.45E-01	-7.38E-01	1.68E+02	1.04E+04	1.33E+02	1.76E+04	1.67E+01
100	100	100	75	100	100	100

Wafer 9

Die Position	N+ Sht R(Ohms)	P+ Sht R(Ohms)	Poly Sht R(Ohms)	Poly Cd(um)	Poly Comb Lkge(Amps)	Poly serp R(Ohms)
3,2	36.78983834	52.46543779	20.95852535	1.955807089	1.76E-11	8.26E+04
8,2	35.54272517	50.59907834	20.04608295	3.19632425	1.73E-11	1.17E+05
6,3	3.41E+01	49.35483871	20.15668203	3.265382488	1.68E-11	1.01E+04
4,3	34.29561201	49.56221198	19.38248848	3.090514895	1.74E-11	7.88E+04
Mean	35.17898383	50.49539171	20.1359447	2.877007181	1.7275E-11	72125
Stddev	1.251435926	1.421679525	0.646230188	0.618329449	3.40343E-13	44777.77537
Min	34.08775982	49.35483871	19.38248848	1.955807089	1.68E-11	10100
Max	36.78983834	52.46543779	20.95852535	3.265382488	1.76E-11	117000
%Yield	100	100	100	100	100	100

Poly Cnt Chain R(Ohms)	M1 Sht R(Ohms)	M1 CD(um)	M1 Comb Lkge(Amps)	M1 Serp R(Ohms)
2.19E+03	49.84655636	3.906892255	0.1	51
2.16E+03	49.39340585	3.886380382	3.33E-11	98.3
1.25E+10	48.03395431	3.947729848	3.20E-11	96
5.48E+03	47.5808038	4.126280406	4.93E-02	66
3.28E+03	48.71368008	3.966820723	3.27E-11	77.825
1908.201597	1.078713984	0.109322034	9.19239E-13	23.1586377
2160	47.5808038	3.886380382	3.2E-11	51
5480	49.84655636	4.126280406	0.1	98.3
75	100	100	50	100

N Vth(V)	P Vth(V)	N+ Cnt R(Ohms)	N+Cnt Chain R(Ohms)	P+ Cnt R(Ohms)	P+ Cnt ChainR(Ohms)	Poly Cnt R(Ohms)
0.589	-0.767	60.2	8.07E+03	144	1.69E+04	7.43
0.63	-0.78	91	1.19E+04	91	1.35E+04	7.76
0.556	-0.753	81.5	1.23E+04	31.8	6.17E+03	859
0.563	DNT	59.6	9.56E+03	24.4	6.31E+03	9.32
0.5845	-0.766666667	73.075	10457.5	72.8	10720	8.17
0.033491292	0.013503086	15.70167189	1998.438974	56.04831249	5356.348259	1.009504829
0.556	-0.78	59.6	8070	24.4	6170	7.43
0.63	-0.753	91	12300	144	16900	9.32
100	100	100	100	75	100	75

Online Resources

- **Runsheet**
  http://www.mirc.gatech.edu/internal/cmostools/processtrack/index.php?runsheet=1&node=1
- **Test Data**
- http://cmos.mirc.gatech.edu/baselines/1.3um/flow.php
- **Processing Forum**
- http://cmos.mirc.gatech.edu/forum/viewforum.php?f=2
- **Project Reports**
- http://cmos.mirc.gatech.edu/group/projects/

Preparation

Prior this run 5 major equipment related issues have been identified as the possible causes for low yields from our previous CMOS runs and been corrected

1. ICP processing selectivity between SiO_2 and Si was reduced to 1:1 (previously was ~11:1)--→Switch to RIE machine;
2. Strong ICP power may cause plasma damage to the gate area--→Use a machine which can apply lower ICP power (STS ICP;
3. Polysilicon grain size was too big--→Clean the tube right before the deposition;
4. Aluminum grain size was too big at normal deposition rate--→Use very slow deposition rate;
5. Cross contamination from other non CMOS compatible sources--→Need to form a processing committee to monitor and control the contamination issue.

Challenges

- Man Power
  - *Need a full time junior engineer, PhD students, and some coop students*
- Infrastructure Support
  - *Consider CMOS processing as the general processing support in the Cleanroom*
  - *Emphasize the importance of the device processing*
  - *Provide better equipment support*

The End